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23 Reply Brief 11-503 OK

In re application of:

Akira TSUKIHASHI

Serial No: 09/476,862

Filed: January 3, 2000

For: DATA PROCESSING CIRCUIT FOR TEMPORARILY SUSPENDING DATA RECORDING ONTO A DISK (As Amended)

Art Unit: 2655

Examiner: G. Patel

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REPLY BRIEF

Applicant has received an Examiner's Answer (Paper No. 22) with a mailing date thereon of August 22, 2003. On page 5 which restates the reason for rejection of claims 3-12 over the prior art, and again in the section entitled "(11) Response to Argument" which begins at the bottom of page 9, the Examiner sets forth certain new arguments. Applicant is filing this Reply Brief in order to address such arguments.

The Examiner's Answer states that because all claims stand or fall together, certain limitations which Applicant has argued with respect to claim 3 are not present in independent claim 7. Nevertheless, the paper goes on to argue that the features defined by these limitations, relating to a write-once disk and synchronization of recording data, are disclosed or suggested by the art, including particularly Shinada.

However, Applicant has maintained, and continues to maintain, that the basic combination in accordance with the invention as defined in claim 7 is patentable over the attempted combination of Shinada and Landry. In rejecting claim 7 (as well as claim 3) on the combination of those references, it is stated in the Examiner's Answer that Shinada does not specifically disclose how his system is suspending operation of the data processing circuit or the details of the suspension circuit and data being placed in a suspended state by interrupting the power supply or by halting an operation clock to the extent claimed. However, Landry is said to clearly disclose the data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock. It is further stated that both Shinada and Landry are interested in controlling the recording operation of the data and avoiding wrong data recording by checking the data content against some reference point [such as threshold or fixed volume of data] and controlling the recording operation. It is further stated in the Examiner's Answer that both references are aware that most of the data processing systems are interrupt driven and need to store data in the buffer because of interrupts that inherently arise from time to time. The Examiner's Answer therefore concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided Shinada with details of controlling the data recording by halting the system clock as disclosed by Landry, because doing so would have provided a mechanism for localizing an error or fault on the spot and easily correcting it.

However, as Applicant has previously pointed out, Shinada merely discloses intermittently writing into a disk. There is no reference to halting the data processing circuit.

In the case of the present invention, the operation of a data processing circuit is placed in a suspended state by interrupting the power supply to the data processing circuit whereby halting the supply of a data clock to the data processing circuit. Consequently, power consumption can be reduced. It is not a feature of the present invention to simply interrupt the operation when there is no data. The method described in Shinada is a thermal magnetic recording method adopted to a rewritable disk. Although not specifically recited in claim 7 as in claim 3, the present invention involves a write-once disk in which recorded data cannot be erased. The configuration is achieved in which the recorded data is read out and new data is written successively, starting at the address of the last recorded data. Shinada can rewrite on the disk and does not show or suggest such configuration in accordance with the invention.

Further in Shinada, data is reproduced from a disk and data is written onto the same disk. Specifically, data is read out from a disk and is output via a buffer. At this time, data output from the buffer is performed at a lower rate than data reading from the disk. Therefore, when recording data from the disk, the amount of data stored in the buffer gradually increases. Then, when the amount of data stored in the buffer reaches a predetermined level, data reading from the buffer is stopped. When writing data is written onto the disk via the buffer, on the other hand, data writing onto the disk is performed at a higher rate than data writing onto the buffer, so that the amount of data stored in the buffer gradually decreases. Then, when the amount of data stored in the buffer is below the predetermined level, data writing onto the disk is stopped.

In Shinada, data reproduction from the disk and data recording onto the disk are alternately performed. Although Shinada describes that data recording is performed intermittently in a manner such that data discontinuity can be avoided,

there is no detailed description of how data is recorded after resumption of recording. Shinada also describes interruption of reproducing when an abnormality such as a track jump is detected. In such case, however, write retry is performed using data stored in the buffer. Thus, it is supposed that in Shinada the recorded data is overwritten to some extent, and that rewriting is started from the second section at which recording was performed without problems.

In the case of the present invention, on the other hand, data already stored in the disk is read, and data is additionally written on the disk in synchronism with the read data. In this manner, additional data write is enabled without generating gaps, even on a write-once disk such as a CD-R. Such a configuration is not disclosed or suggested by Shinada.

Although the Examiner has suggested that additional data write is also performed in Shinada, it appears that Shinada contains no description concerning additional writing as claimed in the present invention.

Shinada is capable of data recording during data reproduction, and reading and writing with regard to the disk are alternatively performed. In the case of the present invention, however, in order to record data continuously to data recorded immediately before interruption of recording, the timing for additional data write onto the disk is established. Therefore, data which is already recorded is reproduced.

Claim 7 defines a recording data processing circuit which includes a buffer memory, a data processing circuit, a system control circuit and a writing circuit. As defined in the last paragraph of claim 7, the system control circuit "suspends operation of the data processing circuit and writing of the recording data onto the disk by the writing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases

suspension of the operation of the data processing circuit to resume writing of the recording data onto the disk by the writing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock". Therefore, claim 7 clearly distinguishes patentably over any teaching or suggestion which Shinada may make.

With respect to the combination of Landry with Shinada in order to disclose or suggest the present invention, Applicant has previously pointed out that Landry merely discloses putting a slave CPU in a sleep state when the data on the bus is not for that CPU. Landry nowhere mentions or suggests turning ON/OFF the operation of the data processing circuit based on the storage capacity of the buffer memory. In the case of the present invention, operation is suspended by interrupting the power supply or halting the supply of an operation clock when buffer underrun occurs. Therefore, the attempted combination of Landry with Shinada does not disclose or suggest the present invention as defined, for example, in independent claim 7.

As noted above, the Examiner's Answer maintains that the limitations with respect to a write-once disk and synchronization of the recording data which are set forth in claim 3 but not specifically in claim 7 are nevertheless disclosed or suggested by Shinada. However, the writable and reproducible optical disk and the hybrid disk partially including a data recording region which are described in Shinada are recordable by way of thermo-magnetic recording. These disks of Shinada are not write-once as a CD-R. Furthermore, Shinada makes no reference to using reproduced data to perform synchronization.

Again, claims 3-12 are submitted to clearly distinguish patentably over the attempted combination of Shinada and Landry. It is respectfully urged to the Board that all of the claims presented in this Appeal should be allowed.

This Reply Brief is submitted herewith in triplicate.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: October 20, 2003

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